

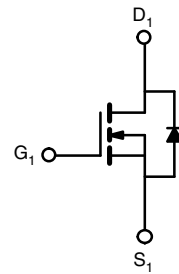
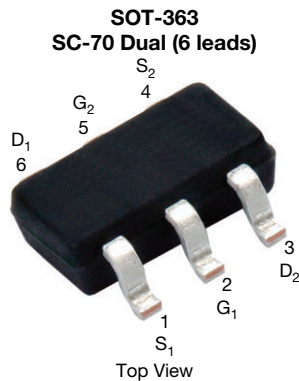
## Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	20
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.415
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 2.5 V	0.600
I <sub>D</sub> (A)	0.78
Configuration	Dual
Package	SC-70

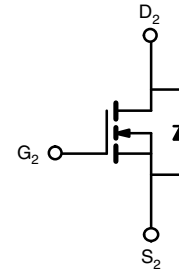
### FEATURES

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- AEC-Q101 qualified <sup>c</sup>
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


N-Channel MOSFET



N-Channel MOSFET

**Marking Code:** 9P

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	20	V
Gate-Source Voltage		V <sub>GS</sub>	± 12	
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	0.78	A
	T <sub>C</sub> = 125 °C		0.45	
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	0.54	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	3	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	3.5	
Single Pulse Avalanche Energy		E <sub>AS</sub>	0.6	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	0.43	W
	T <sub>C</sub> = 125 °C		0.14	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>b</sup>	R <sub>thJA</sub>	460	°C/W
Junction-to-Foot (Drain)		R <sub>thJF</sub>	350	

### Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		20	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		0.6	1.0	1.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 4.5 V	V <sub>DS</sub> ≥ 5 V	0.8	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 0.66 A	-	0.200	0.415	Ω
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 0.66 A, T <sub>J</sub> = 125 °C	-	-	0.594	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 0.66 A, T <sub>J</sub> = 175 °C	-	-	0.698	
		V <sub>GS</sub> = 2.5 V	I <sub>D</sub> = 0.4 A	-	0.250	0.600	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A		-	1.1	-	S
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 10 V, f = 1 MHz	-	50	75	pF
Output Capacitance	C <sub>oss</sub>			-	21	28	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	9	15	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 4.5 V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.2 A	-	0.7	1.2	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	0.1	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	0.1	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		4.5	9.1	13.7	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 20 Ω I <sub>D</sub> ≅ 0.5 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		-	10	15	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	22	30	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	20	28	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	18	25	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	3	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 0.5 A, V <sub>GS</sub> = 0		-	0.85	1.2	V

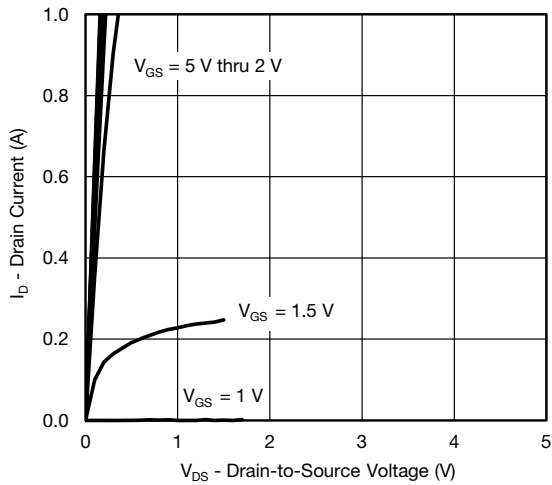
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

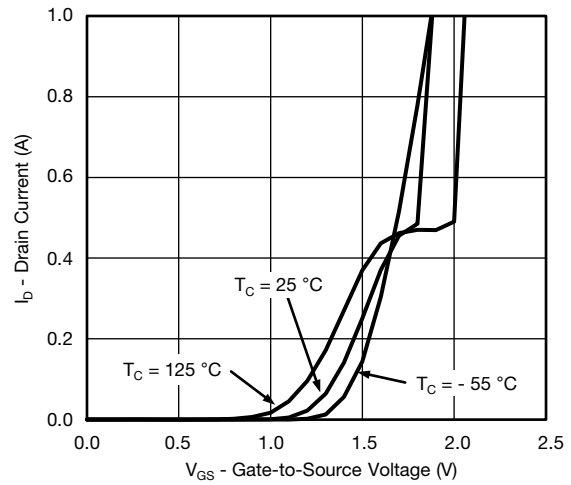
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



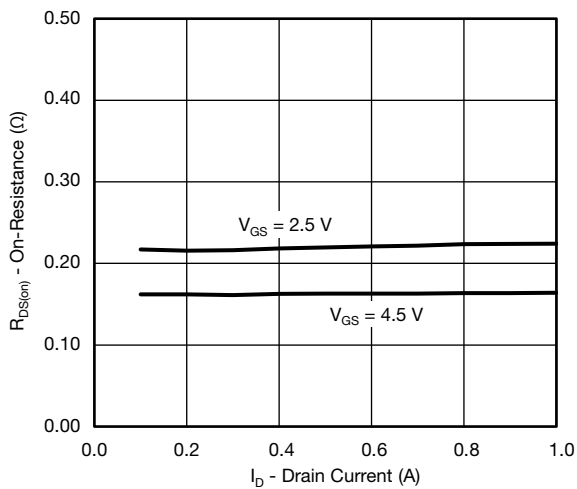
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



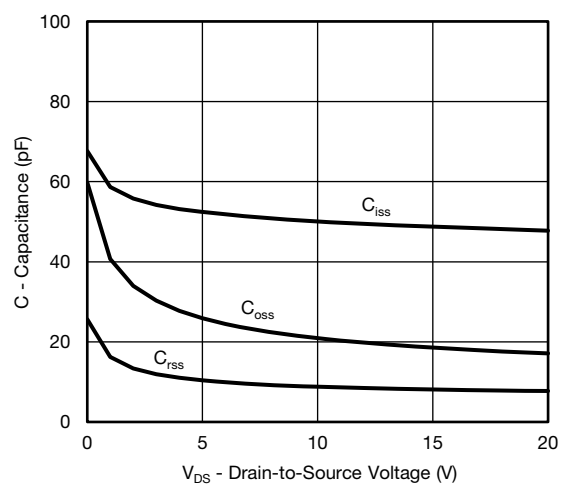
**Output Characteristics**



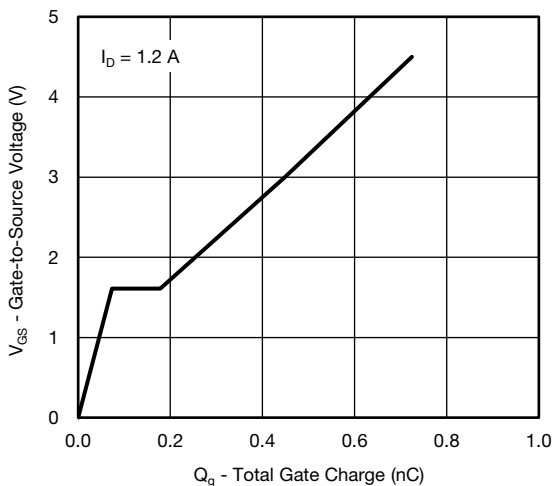
**Transfer Characteristics**



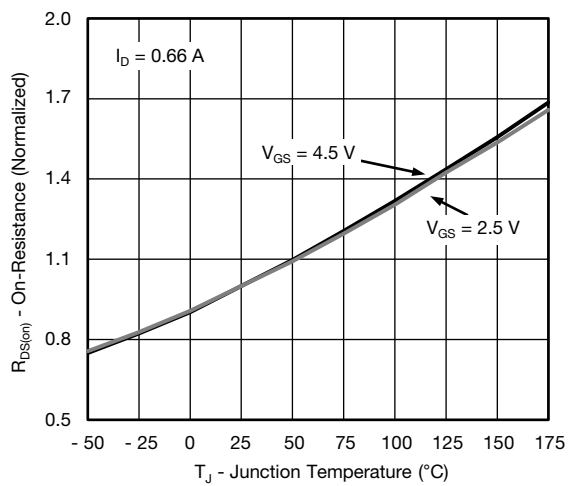
**On-Resistance vs. Drain Current**



**Capacitance**



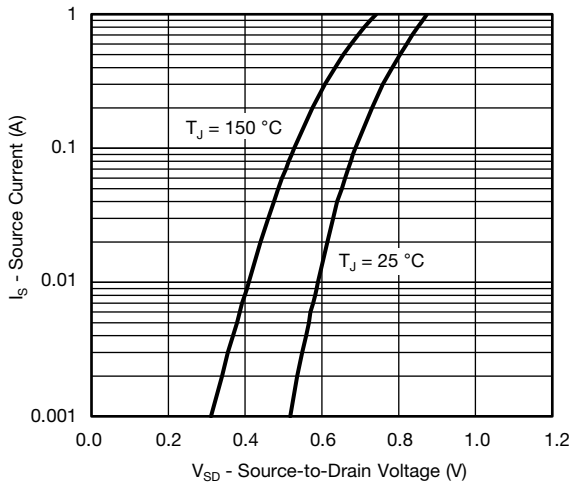
**Gate Charge**



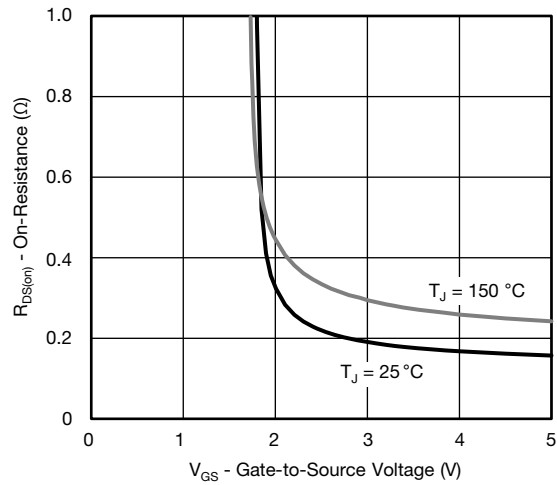
**On-Resistance vs. Junction Temperature**



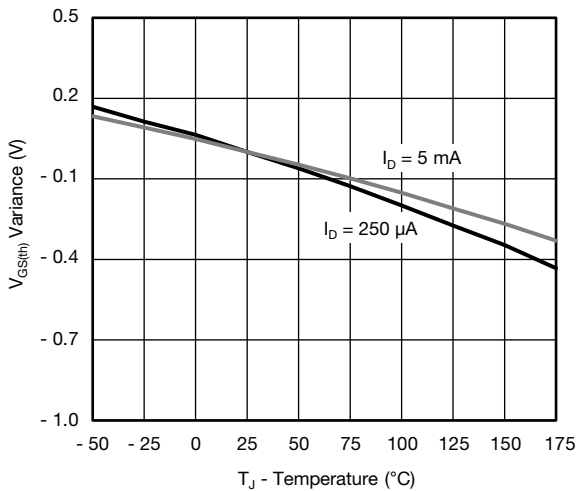
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



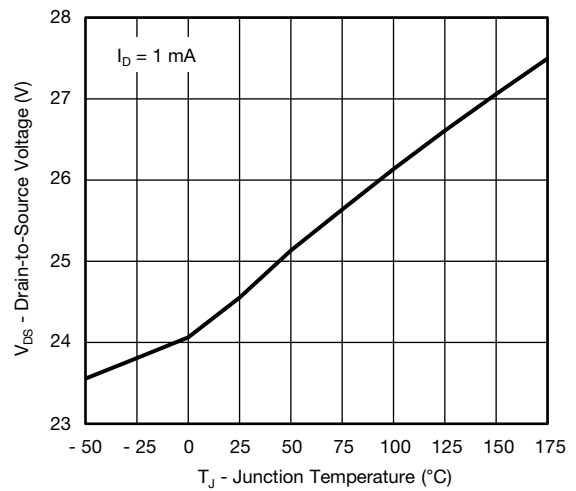
Source Drain Diode Forward Voltage



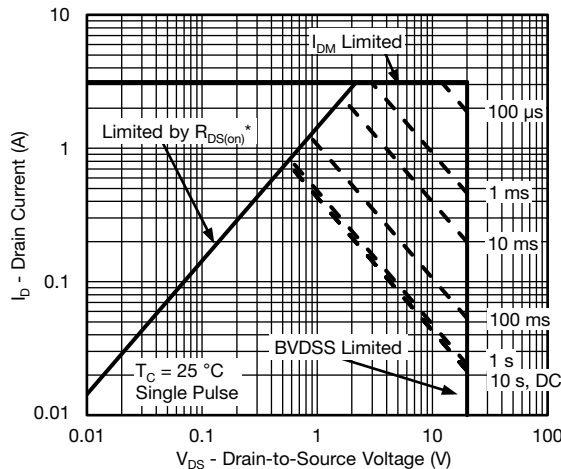
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



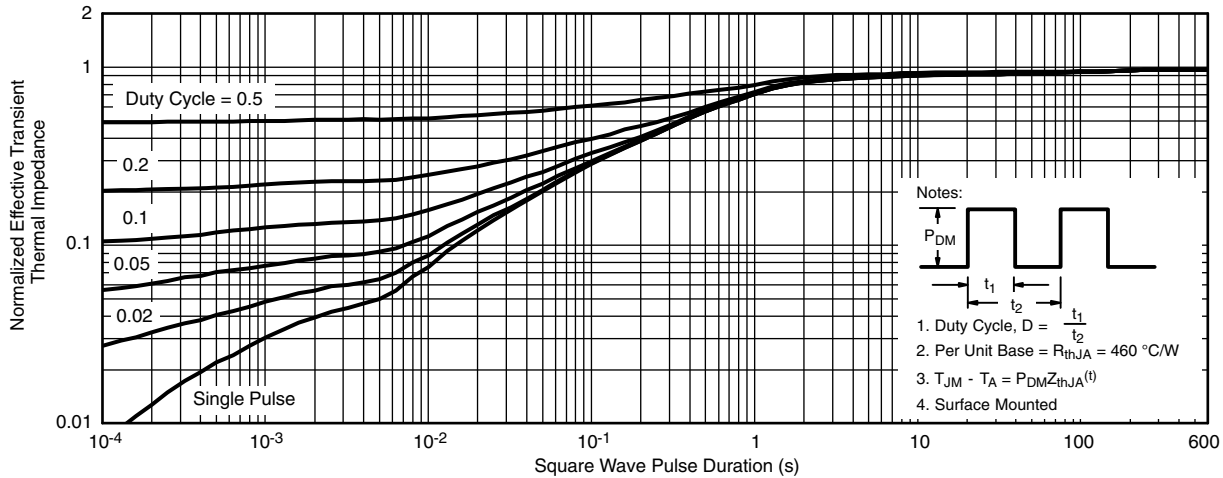
Drain Source Breakdown vs. Junction Temperature



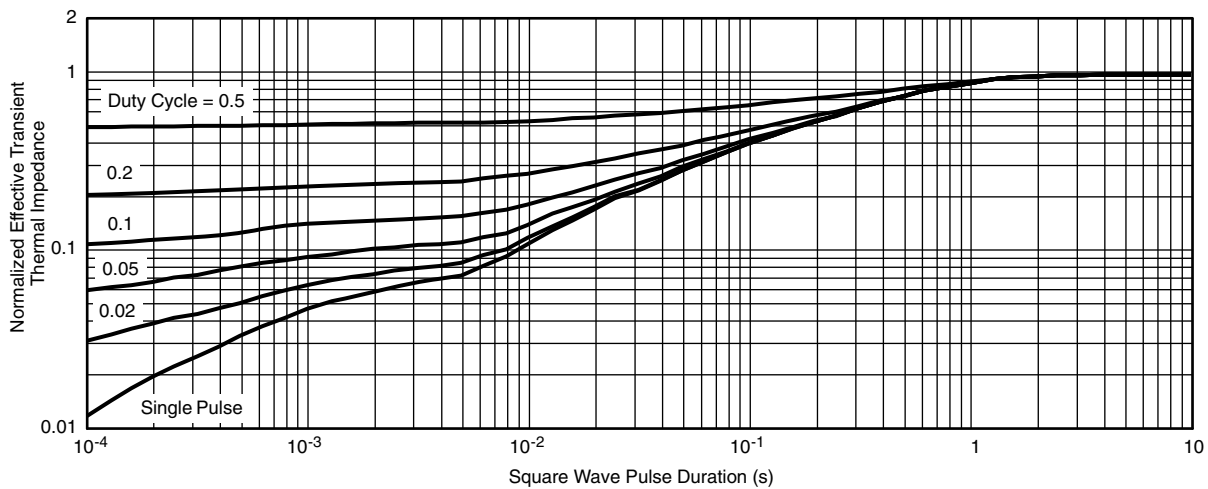
Safe Operating Area



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62977](http://www.vishay.com/ppg?62977).



**SC-70: 6-LEADS**



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A <sub>1</sub>	-	-	0.10	-	-	0.004
A <sub>2</sub>	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01						
DWG: 5550						

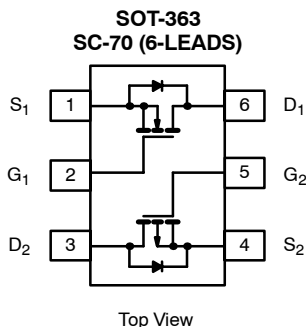
## Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

### INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

### PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.



**FIGURE 1.**

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

### BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power

applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

### EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

### THERMAL PERFORMANCE

#### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The “foot” is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

#### Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical  $R\theta_{JA}$  for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

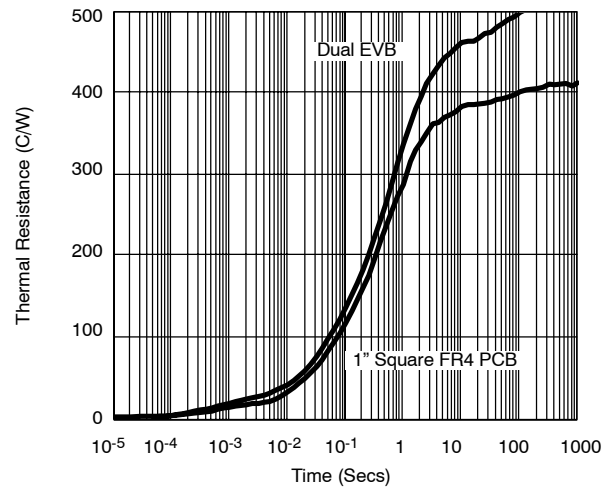
<b>SC-70 (6-PIN)</b>	
<b>Room Ambient 25 °C</b>	<b>Elevated Ambient 60 °C</b>
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^{\circ}C - 25^{\circ}C}{400^{\circ}C/W}$	$P_D = \frac{150^{\circ}C - 60^{\circ}C}{400^{\circ}C/W}$
$P_D = 312 \text{ mW}$	$P_D = 225 \text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

**Testing**

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of  $R\theta_{JA}$  for the dual 6-pin SC-70 are as follows:

<b>LITTLE FOOT SC-70 (6-PIN)</b>	
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518 °C/W
2) Industry standard 1" square PCB with maximum copper both sides.	413 °C/W



**FIGURE 2.** Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

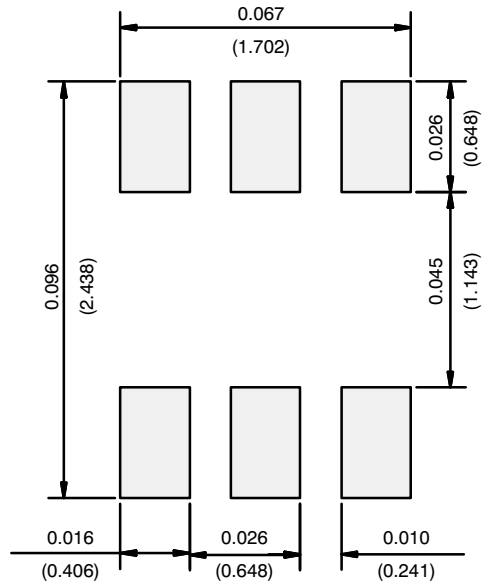
The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

**ASSOCIATED DOCUMENT**

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (<http://www.vishay.com/doc?71334>).



## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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